Code :R7310404

R7

III B.Tech I Semester(R07) Supplementary Examinations, May 2011
DIGITAL IC APPLICATIONS
(Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Draw the logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate.
   (b) Show the transistor circuit for this gate and explain the operation with the help of function table.
2. (a) Draw the circuit diagram of two-input 10K ECL OR gate and explain the circuit.
   (b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00.
3. (a) Explain the behavioral design model of VHDL.
   (b) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.
4. (a) Using two 74138 decoders design a 4 to 16 decoder.
   (b) Write a data flow style VHDL program for the above design.
5. Design a 10-4 encoder with inputs 1 out of 10 and outputs in BCD provide the VHDL code in data flow model.
6. Write a behavioral code for comparing a 16 bit signed and unsigned integers.
7. Explain the timing specifications of PLD with an appropriate diagram. Give the VHDL code for PLD.
8. (a) Draw the block diagram of SSRAM and explain each block precisely.
   (b) Explain the read timing behavior with a pipe lined outputs in SSRAM.

⋆ ⋆ ⋆ ⋆ ⋆